PATENT ABSTRACTS OF JAPAN

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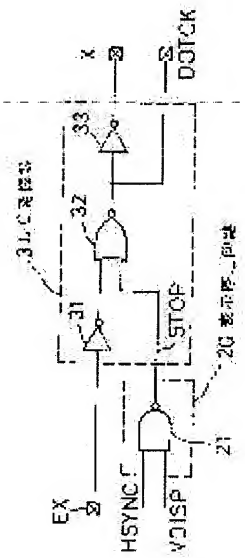
(54) DISPLAY CONTROL CIRCUIT



(57)Abstract:
PURPOSE: To save electric power by stopping the generation of a dot clock signal in a period wherein a dot clock signal needs to be oscillated, i.e. a vertical blanking period.
CONSTITUTION: This display control circuit is equipped with an LC oscillator 3 which generates the dot clock signal DOTCK used to display characters and a display stopping circuit 20 which outputs an oscillation stop signal STOP to the LC oscillator 3. The display stopping circuit 20 inputs two signals, i.e. horizontal synchronizing signal HSYN and vertical display signal VDISP and outputs the display stop signal STOP according to the output of a NAND circuit 21 which NANDs those input signals. The output of the dot clock signal DOTCK is therefore stopped in the vertical blanking period. Consequently, the power consumption is reduced.